Remarks

The evidence of record demonstrates that the '178 reference, upon which all rejections are based, fails to disclose and further teaches away from the claimed invention. Specifically, the '178 reference is directed to a memory control approach involving a preconditioning step that first discharges cells, prior to charging them, which causes performance issues with such memory cells as discussed in the background of the instant application. The following addresses these and other matters in greater detail.

In the non-final Office Action dated October 29, 2008, the following rejections were indicated: claims 1, 2, 5, 6, 14-16 and 21 were rejected under 35 U.S.C. § 102(b) over Krishnamurthy (U.S. Patent No. 6,233,178); claims 3, 7-9, 11, 17 and 20 were rejected under 35 U.S.C. § 103(a) over Krishnamurthy in view of Guliani (U.S. Patent No. 6,366,497); claims 4 and 10 were rejected under 35 U.S.C. § 103(a) over Krishnamurthy in view of Guliani and further in view of Takahashi (U.S. Patent No. 6,639,849); and claims 12-13 and 18-20 were rejected under 35 U.S.C. § 103(a) over Krishnamurthy in view of Guliani and further in view of Kurihara (U.S. Patent Pub. 6,791,880). Applicant respectfully traverses all claim rejections, and in this discussion set forth below, does not acquiesce to any rejection or averment in this Office Action unless Applicant expressly indicates otherwise.

All of the claim rejections are improper because the Office Action has misconstrued both the order and function of the cited flash memory charging and erasing steps in the '178 reference, upon which all claim rejections are based. The claimed invention is directed to charging/programming memory devices as a first step, prior to discharging/erasing the memory devices (*see*, *e.g.*, claim 1). In contrast, the cited '178 reference discloses an approach that is nearly opposite to the aforesaid steps by first discharging (programming) memory with a preconditioning write step, prior to charging (erasing) the memory as an erase step. Not only are these steps out of order as relative to the claimed invention (discharging, prior to charging, rather than charging, prior to discharging), they use opposite functions to respectively erase and charge memory. That is, the '178 reference charges (instead of discharging) the memory cells to erase them, and further discharges (instead of charging) the memory cells to program them.

As consistent with the above, the '178 reference also teaches away from the claimed invention. The discharging and subsequent charging steps of the '178 reference are described in the reference's Abstract and cited column 4, in which flash memory devices are first preconditioned by discharging cells, prior to charging the cells. The erasing step in the '178 reference is further described at column 5:1-3, which indicates that "[d]uring the erase step 320, all cells 120 within a sector are erased, setting cells 120 within the sector to their charged state" (*i.e.*, the cells are erased by charging). This is consistent with the discussion at page 3 of the Office Action, which states that the '178 reference "discharges cells as taught in Col 4 lines 43-45" as a preconditioning (first) step.

Importantly, the background of Applicant's specification explains, according to the teachings of the '178 reference, various issues with the reference's charging and discharging approach (see paragraphs 0006 and 0007 of the Background of the instant application). Specifically, the '178 reference's preconditioning step involves discharging that may result in discharging an already discharged memory cell, which can deteriorate the cell. The claimed invention addresses such problems (*see*, *e.g.*, paragraph 0008) and presents a memory control solution with results that are clearly different than those in the '178 reference. Accordingly, since the '178 reference teaches a memory management approach that causes the problems noted in the background of the instant application, the reference actually teaches away from the asserted combination of references.

The M.P.E.P. and the applicable U.S. Supreme Court law requires that the claim be considered "as a whole" (35 U.S.C. §103(a)), while taking into consideration the problem(s) being addressed by the claimed invention and any unexpected results. Thus, Supreme Court in *KSR* reaffirmed the familiar framework for determining obviousness as set forth in *Graham v. John Deere Co.* (383 U.S. 1, 148 USPQ 459 (1966)), and stated that, "when the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious." The Court further tied in the relationship between the teach-away standard and demonstrating unpredictable results. "The fact that the elements [in *Adams*] worked together in an unexpected and fruitful manner supported the conclusion that Adam's design was not obvious to those skilled in the art." *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742

(2007). Accordingly, the '178 reference not only fails to disclose or contemplate the claimed invention, it further teaches away from the claimed invention.

Applicant notes that the '178 reference may have presented confusion regarding the cited steps, as a typographical error at column 4:33-37 mistakenly switches the erasing and programming steps 320 and 330 of FIG. 3. It appears that the Examiner may also be misinterpreting claim 1, wherein the first-listed step is prefaced by the term "before," such that the second listed step occurs first. That is, the block programming step (charging) is carried out before the block erasing step (discharging).

In view of the above, the cited portions of the '178 reference fail to disclose, teach or suggest limitations in both of independent claims 1 and 5. As the rejections of claims 2-15 and 21 rely upon the misapplied portions of the '178 reference, all of these claim rejections are improper and should be removed.

Applicant notes that independent claim 16 has been amended in a manner consistent with the specification and the above discussion, in which the claimed block programming step involves charging the cells, which ensures that the cells are charged prior to a block discharge (erase), which can help to mitigate cell damage as described in the background of the instant application. Accordingly, Applicant submits that the cited portions of the '178 reference fail to disclose the limitations of claim 16 as amended, and requests that the rejections of claim 16 and of claims 17-20 (which depend from claim 16) be removed.

In view of the above, Applicant believes that further discussion of the Section 103 rejections is unnecessary. However, Applicant submits that the proposed combinations of references cannot stand, as the resulting structure would not correspond to the claimed invention (per the above), and would render the '178 reference inoperable for its purpose (as relevant to replacing its discharging/charging steps with the steps as claimed), which contradicts the M.P.E.P. and relevant law. Applicant therefore submits that the Section103 rejections are also improper for these reasons.

Applicant has made stylistic changes to certain claims (*e.g.*, change the term "arranged" to "configured"). Applicant believes that these amendments do not change the scope of the claims.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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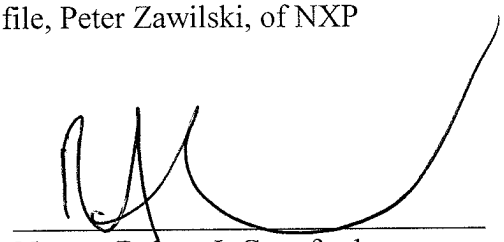
By: 

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